

Look-ahead approach tames large FPGA counters

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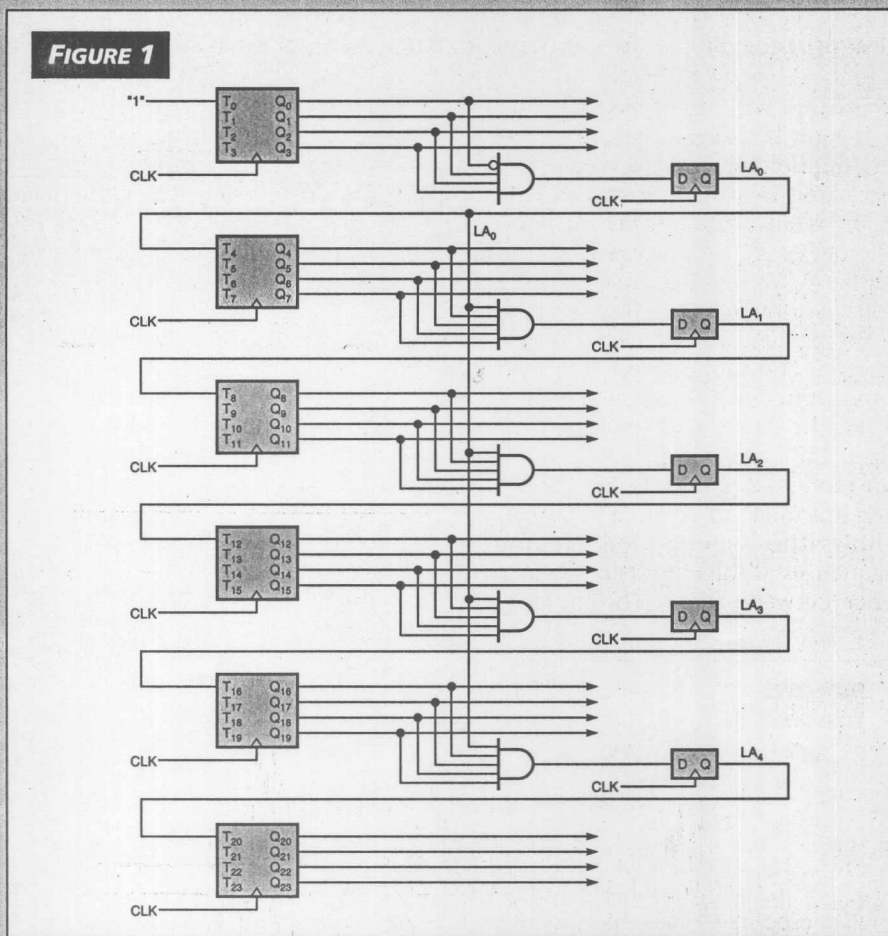
The T flip-flops and look-ahead technique in Fig 1 allow you to program large, fast counters in FPGAs (field-programmable gate arrays). The look-ahead technique detects when the least-significant 4-bit block (Q_3 through Q_0) has the value 1110. The technique registers this event in a D flip-flop to create the look-ahead signal (LA_0 through LA_4). The look-ahead bit indicates that the most-significant counter bit should toggle at the next clock edge. Note: The look-ahead circuitry detects 1110₂ and not 1111₂ because the D flip-flop introduces one cycle of latency.

T flip-flops obviate the n -bit-wide OR gate that an n -bit counter would need if you used a conventional sum-of-products architecture. Otherwise, you need to use slower, multiple levels of logic to realize wide logic states in FPGAs.

Similarly, the look-ahead technique avoids the $n-1$ -bit-wide AND gate that an n -bit counter based on T flip-flops requires. Such a wide AND gate would impose an excessive fan-out burden on some of the T flip-flops (Fig 2). For example, in the 24-bit counter in Fig 1, the most highly loaded D flip-flop has a fan-out of 4 instead of 23. (DI #1633)

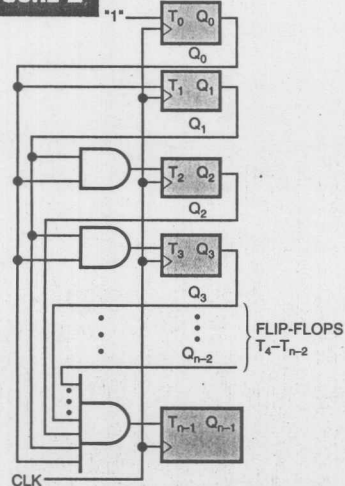
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You can program large, fast counters in FPGAs using T flip-flops and the look-ahead technique.

FIGURE 2



The look-ahead technique avoids wide AND gates and excessive fan-out burdens.

Data

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	CLKOUT	Feedback
1	0	1	0	1	0	1	0	CLK/2	QH
1	1	0	0	1	1	0	0	CLK/4	QH
1	1	1	1	0	0	0	0	CLK/8	QH
1	1	1	1	1	1	1	1	CLK/16	QH

Data

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	CLKOUT	Feedback	Duty Cycle
1	0	0	0	1	0	0	0	CLK/4	QH	25%
1	1	0	0	1	1	0	0	CLK/4	QH	50%
1	1	1	0	1	1	1	0	CLK/4	QH	75%
1	1	0	0	0	0	0	0	CLK/8	QH	25%
1	1	1	1	0	0	0	0	CLK/8	QH	50%
1	1	1	1	1	1	0	0	CLK/8	QH	75%